

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
)
Tsutomu TEZUKA et al.)
) Group Art Unit: Not assigned
Serial No.: Not Yet Assigned)
) Examiner: Not assigned
Filed: July 29, 2003)
)
For: SEMICONDUCTOR DEVICE)
MANUFACTURING METHOD)

**Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450**

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§1.56 and 1.97(b), applicants bring to the Examiner's attention the documents listed on attached Form PTO-1449. Copies of the listed documents are attached. Applicants respectfully request that the Examiner consider the documents listed on attached Form PTO-1449 and indicate that they were considered by making an appropriate notation on this form.

This Information Disclosure Statement is being filed with the above-referenced application.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and applicants determine that the cited documents do not constitute "prior art" under United States law, applicants

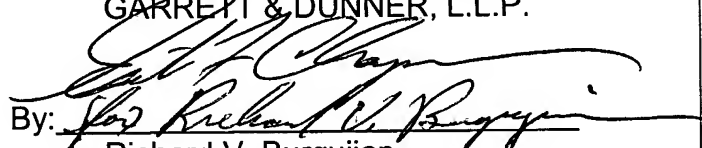
reserve the right to present to the office the relevant facts and law regarding the appropriate status of such documents. Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: July 29, 2003

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Enclosures
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INFORMATION DISCLOSURE CITATION

Atty. Docket No.	04329.3105	Serial No.	
Applicant	Tsutomu TEZUKA et al.		
Filing Date	July 29, 2003	Group:	Not assigned

U.S. PATENT DOCUMENTS

Examiner Initial*	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	T. Mizuno et al., "High Performance Strained-Si p-MOSFETs on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology", IEDM Technical Digest, pp. 934-936 (1999).
	T. Tezuka et al., "Fabrication of strained Si on an ultrathin SiGe-on-insulator virtual substrate with a high Ge fraction", Applied Physics Letters, 79, pp. 1798-1800 (2001).
	F. Y. Huang et al., "High-quality strain-relaxed SiGe alloy grown on implanted silicon-on-insulator substrate", Applied Physics Letters, 76, pp. 2680-2682 (2000).

Examiner	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce